

High-Performance Deformable Mirrors, Driver ASICs and Integration of Both for Space Based Active Optics

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Motivation

- Deformable mirrors (DMs) for many terrestrial and airborne applications need speed, and therefore power. Existing electronics for them (drivers and cabling) are large, heavy and power-hungry.
- Deformable mirrors for space typically do not need terrestrial speed or stroke, but do need a smaller, lighter solution.
- The solution we are working on is to shrink the driver and to eliminate cabling by integrating the driver and DM.

Team

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DMs are needed for Exoplanet Detection

 Exoplanet direct imaging with an adaptive optics (AO) coronagraph requires high-order DMs (typically two, ≥48x48) to improve the contrast between star and planets.



An AO Coronagraph Concept

WFIRST-AFTA Mission Concept

- Traditional DM cabling has 1 wire per actuator plus a number of ground or return wires => thousands of wires.
- Commercial driver electronics are commonly sized for terrestrial use, are too powerful and large for space use.

What do we want in a DM for Exoplanet Imaging from Space?

Number of Actuators Stroke Slew rate RMS Surface Error Actuator Yield Driver Resolution Static and Dynamic Power Mass/No. of Wires Actuator Pitch 48x48 and up ~0.5 µm Very slow <1 nm 100% Compatible with 5 pm The less the better The less the better Free parameter until frozen

Deformable Mirrors (DMs)

• **DMs** have a deformable mirror surface, or **facesheet**, and **actuators**.



• They also have **driver electronics**, and typically have significant cabling between driver and DM.

Coronagraphic Testbed DM and Electronics



The Solution – Integrate the DM and its Driver



8x8 DM/ASIC Assembly for Testing

An Application Specific Integrated Circuit (ASIC) can control the DM. Mating it directly with the DM eliminates the need for large bundles of wires.

Microscale DM-ASIC Architecture



Packaged Deformable Mirrors





8x8 DM

16x16 DM

100% yield has been obtained at the finished DM level for 8x8 and 16x16 DMs.

Packaged ASICs



8x8 ASIC



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Building a 32x32 DM



32x32 actuator array, tested to have 100% actuator yield before attaching facesheet.

Backside of facesheet with posts

32x32 DM with Facesheet Attached



Left: 32x32 DM, finished except for protective cover Right: 32x32 DM, with camera focused on reflection of ceiling lights. This DM has been delivered to JPL but is not yet tested

16x16 DM Interferogram and Influence Function





Zygo interferogram of 16x16 DM with four actuators poked.

Influence function at 0.5 actuator is 0.612 Influence function at 1.0 actuator is 0.040. The tail of the influence function is

different for edge and corner actuators.

16x16 DM Testing – Linearity and Leakage



Gain: 17 nm/volt Stroke error +/- 16nm Open circuit decay rate is 0.43 nm/sec

Summary of 16x16 DM testing

- Gain: 17 nm/volt.
- Stroke has a linear relation up to test limit of 75V (actuator is rated to 80V, or 1.4 µm stroke).
- Decay due to leakage current is 0.43 nm/sec.
- Stability of 0.47 / 1.8 nm (over time @ 12 / 30 V)
- Repeatability (cyclic charge/discharge) of 1.2 nm.
- Hysteresis is normal for the material (PZT).
- Influence function at 0.5 actuator pitch is 0.612.
- Influence function at 1.0 actuator pitch is 0.040.
- Influence function is essentially independent of actuator location, as actuator posts are fabricated monolithically with the facesheet, rather than glued to it.

8x8 DM-ASIC Properties and Test Results

- The DM-ASIC is a switch matrix that connects external high-voltage amplifiers (HVAs) to actuators.
- A control pin selects whether 1 or 8 external HVAs are multiplexed to the actuator array.
- Current ASIC foundry process limits voltage to 40 V; current actuators are rated to 80 V.
- Control resolution: 0.04 mV
- Off leakage current: <4 pA
- Off leakage current at HOLD state: <2 pA (1 nF load)
- Static power dissipation: <4mW (entire 20mm x 20mm ASIC)

Next Steps

- Test the PGA-Packaged ASICs (8x8, 16x16)
- Develop improved connectivity concept
- Package a 32x32 ASIC
- Test 32x32 DM
- Test a combined ASIC/DM
- Develop single-crystal PMN-PT actuator arrays & DMs
- Start ASIC Environmental / Radiation Testing in 2018
- Develop scaling concepts to 48x48 and/or 64x64
- Developing methods to improve mirror surface figure

Manual vs Automated Testing of DMs



- Left: Early testing involved manually pushing wires with sockets onto DM pins.
- Center and right: DM driver board with conventional electronics developed in FY17 will allow automated testing of 8x8 and 16x16 DMs in FY18. Notice how much larger conventional electronics are compared to Microscale DM or ASIC.
- To be developed in FY18: A high-speed computer interface board to host the Microscale ASIC drivers to enable testing of 32x32 DMs.

DM-ASIC Connectivity

- Both the DMs and the ASICs from Microscale are performing well.
- A hot item of discussion now at Microscale and JPL is the best way to provide an non-permanent connection between the DM and the ASIC driver, to test each individually, and to enable mix and match of good drivers and good DMs.
- This is particularly an issue for exoplanet observations, where dimensionalities of 48x48, 64x64 and larger are desired, and yield in the illuminated pupil must be 100%.
- The original concept of indium bump bonding does not provide for easy, non-destructive, disassembly.
- We are currently using pin grid arrays with ZIF sockets, but do not believe this is a long-term or flightworthy solution.
- Connectivity discussions are now focusing on creating a grid of compliant (spring or elastomer) connections.

Single Crystal PMN-PT Stack Actuator DM Development

Innovation

Batch manufacturing of arrays of single crystal PMN-PT stack actuators

Benefits

Improved DM electro-mechanical performance Stable operation at cryogenic temperatures Scalable to 128x128 DMs Flexibility in actuator sizes

Simplified connectivity

No reliance on external vendors

Reduced cost/weight/size/power for space-based DMs

Ultimate Goal: Filling the NASA Technology Gap (Gap ID: CG-3) on DM and associated electronics

Funding Source: NASA SBIR Phase I (June-December 2017, Contract No. NNX17CP52P)

Current Phase I Development Status:

- 1. Have completed Phase I design and device modeling
- 2. Have completed Phase I process development for batch fabricating stack actuator array
- 3. Currently prototyping an actuator array and a 5x5 DM for a Phase I demonstration.
- 4. Phase I will conclude at TRL3 with a hardware delivery of a programmable DM module.





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