Low-Stress Silicon Cladding for Surface Finishing Large UVOIR Mirrors NASA

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Introduction

- In this presentation, I will discuss the status of our silicon cladding development effort, which is based on ion-assisted, physical evaporation (PV)
- The coating area is currently 1.2-meter in diameter and in Phase II, we will demonstrate the process over a larger area (~2.5-m).

What is Silicon Cladding?

- Silicon cladding is a material applied on the surface of a SiC mirror substrate, to provide a better surface to polish and to make it less time consuming to figure
- A 10 to 100-micron silicon layer is typically applied
- Why Silicon? Good material to diamond turn or polish, and the CTE is very close to SiC

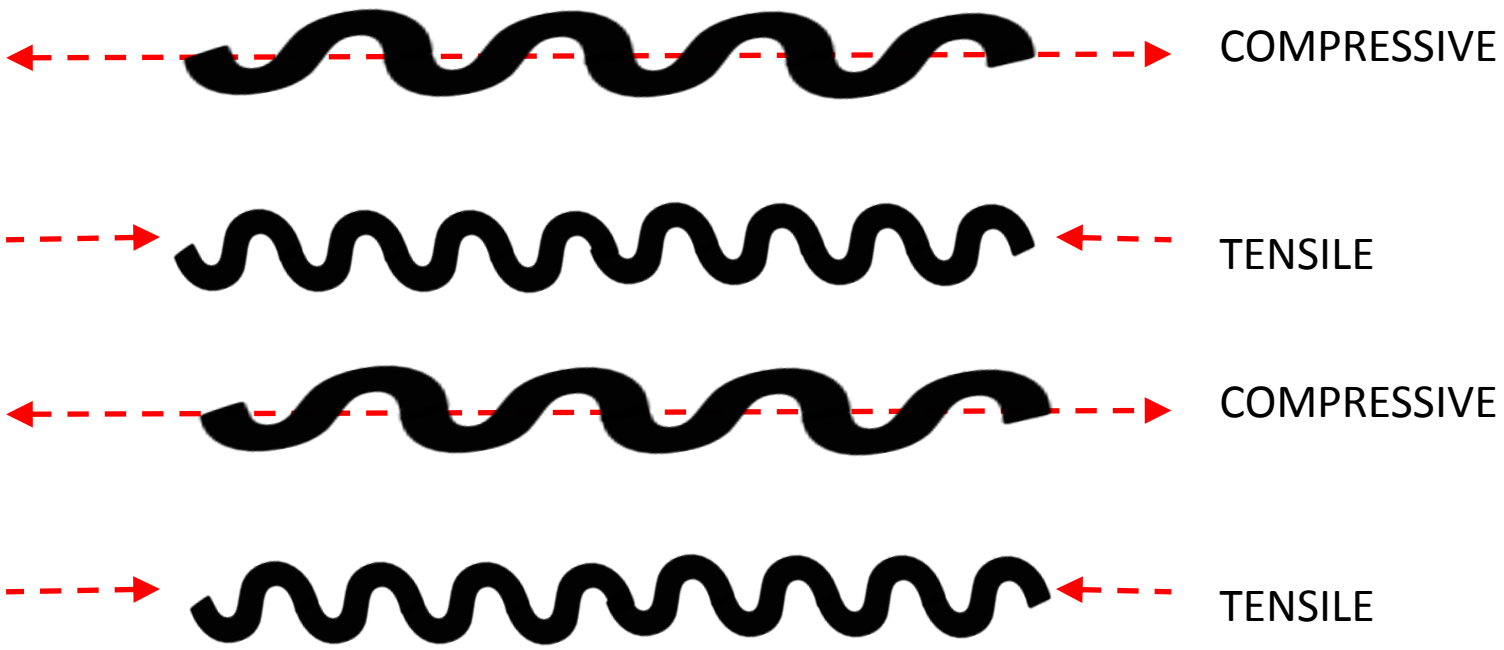
Limitations of commercially available CVD Si Cladding

- Size is currently limited to substrates less than 1-meter
- High temperature process (several hundred degrees C) makes process difficult to scale to larger size
- High temperature limits the type of mirror assembly that may be clad
- Coating stress is relatively high, which can cause bending of lightweight mirrors

Why is a silicon cladding process based on *evaporation* potentially very useful?

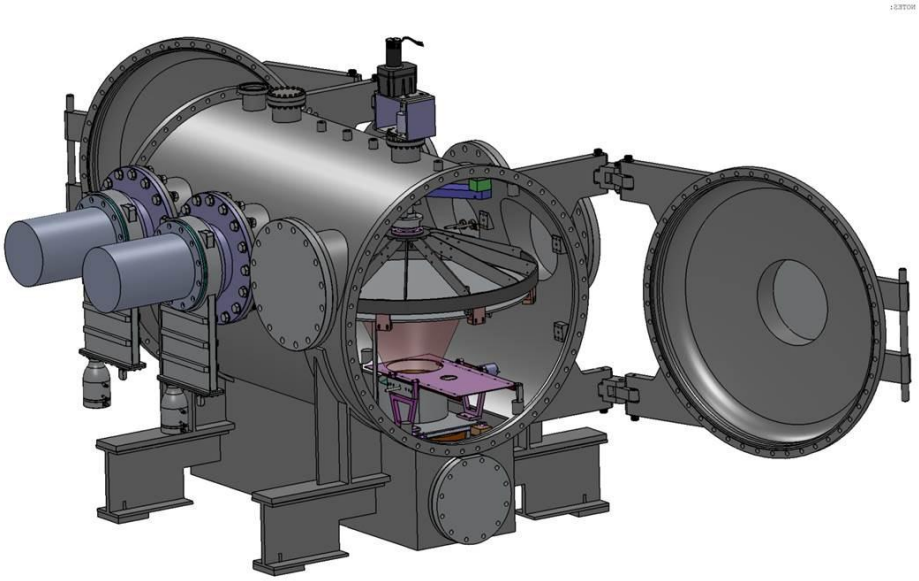
- Process works at temperatures under 100 C and is scaleable to large mirrors (goal is 4-meters+)
- Many silicon carbide technologies produce surfaces that are simply not smooth enough for mirrors, so some type of cladding is needed

ZeCoat's cladding process is based on alternating the sign of the coating stress to yield a near-zero net coating stress.

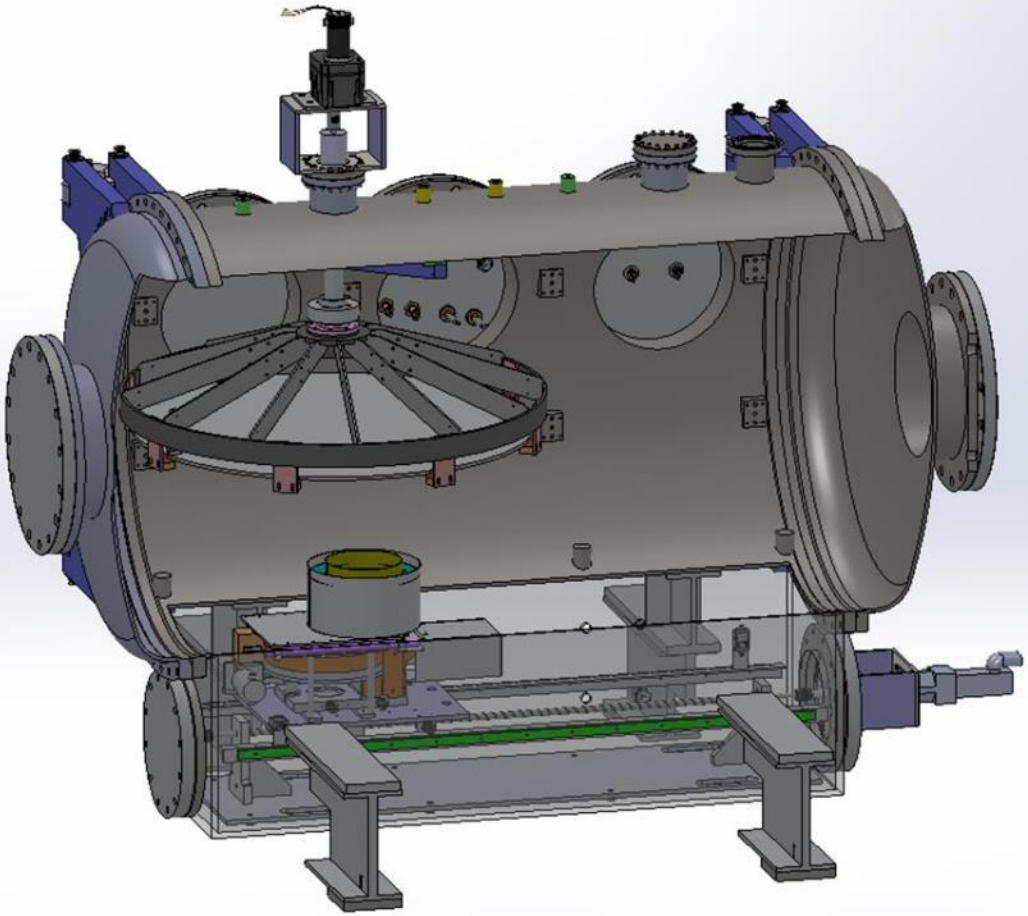


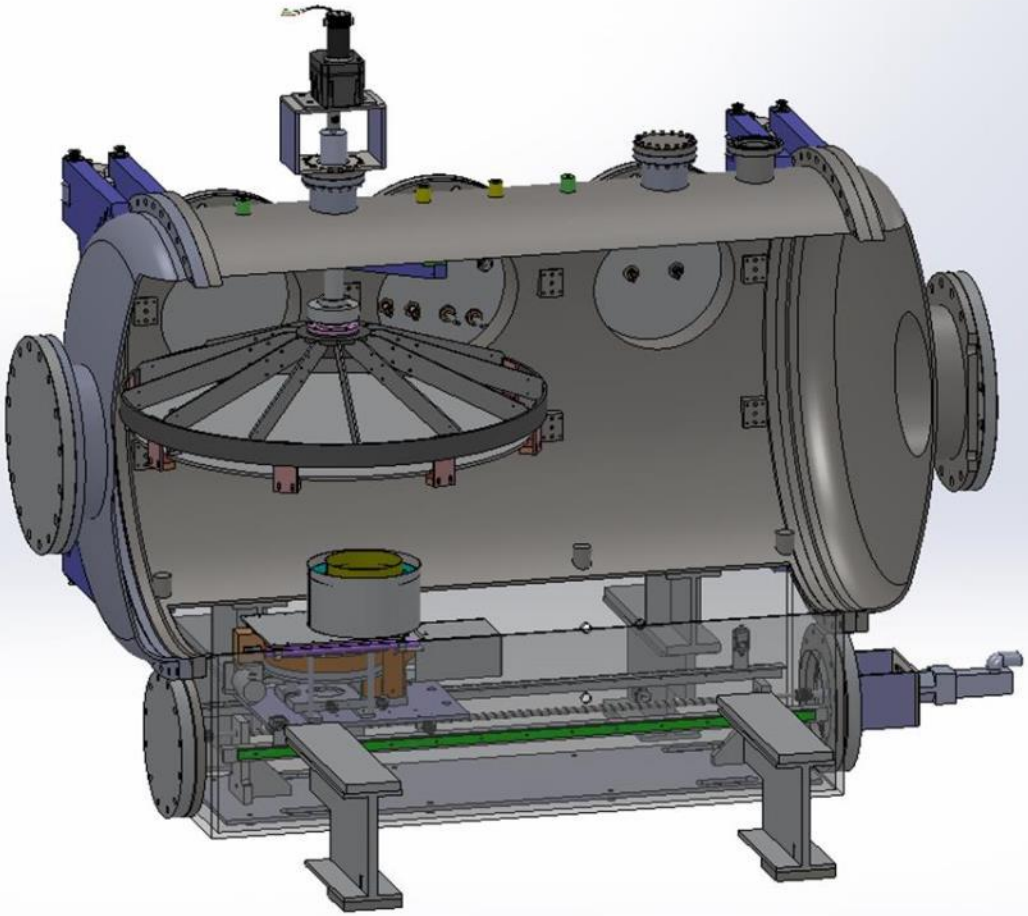
Why not find one set of processing conditions that yields low stress?

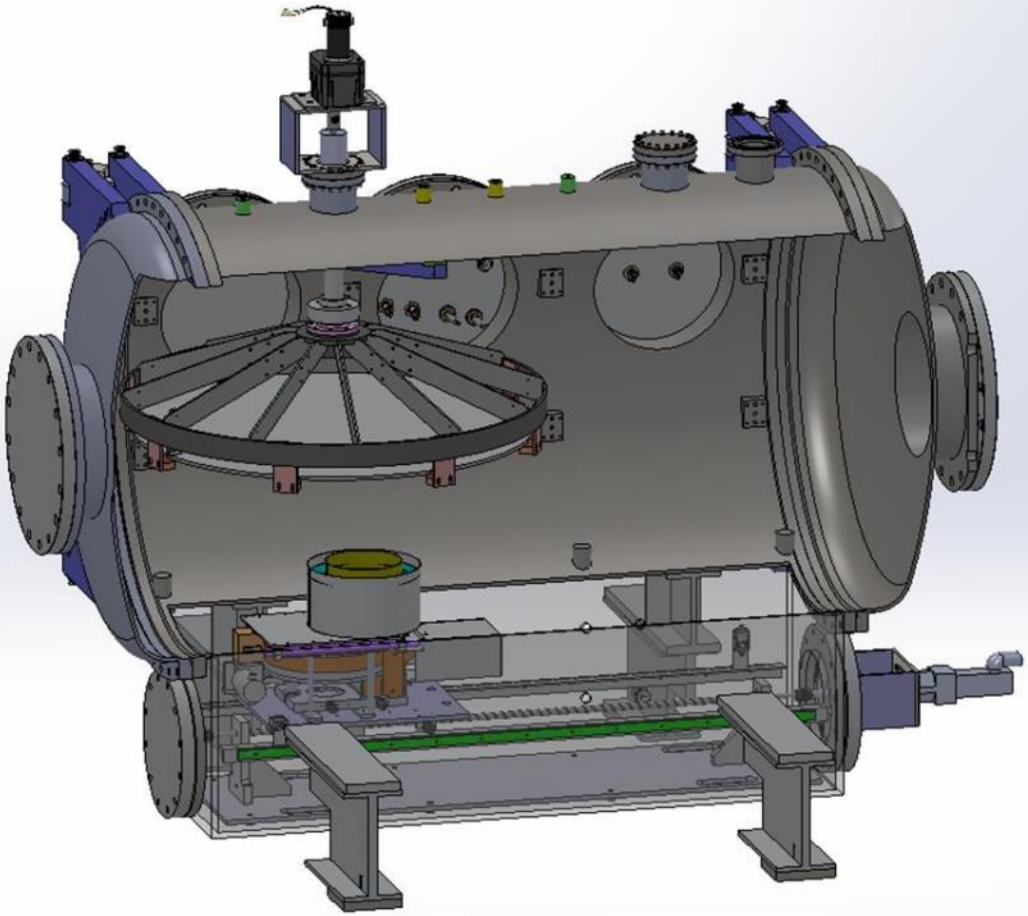
- ANSWER: In previous research, we tried to find one set of processing conditions that yielded low stress but could not demonstrate process repeatability. It appeared that the processing conditions that yield low stress are in a unstable process region. However, we found it less difficult to make layers with consistently high tensile or, high compressive stress and stack them together.

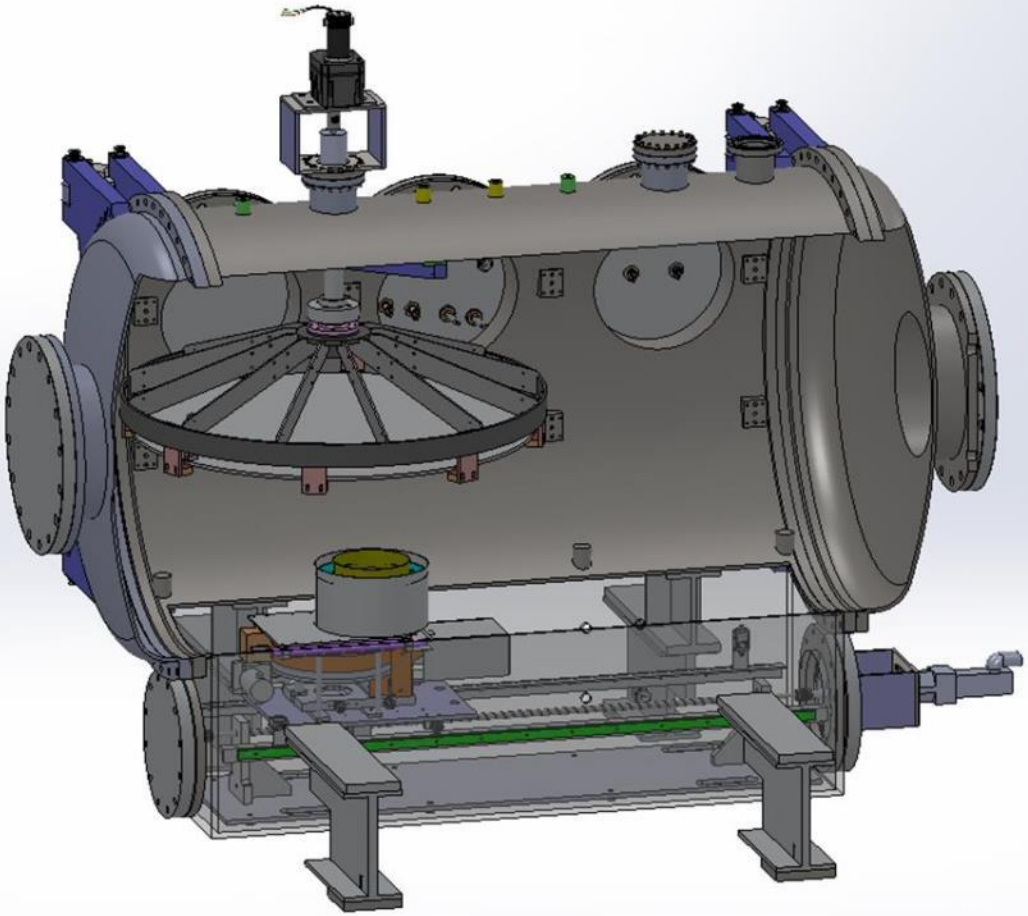


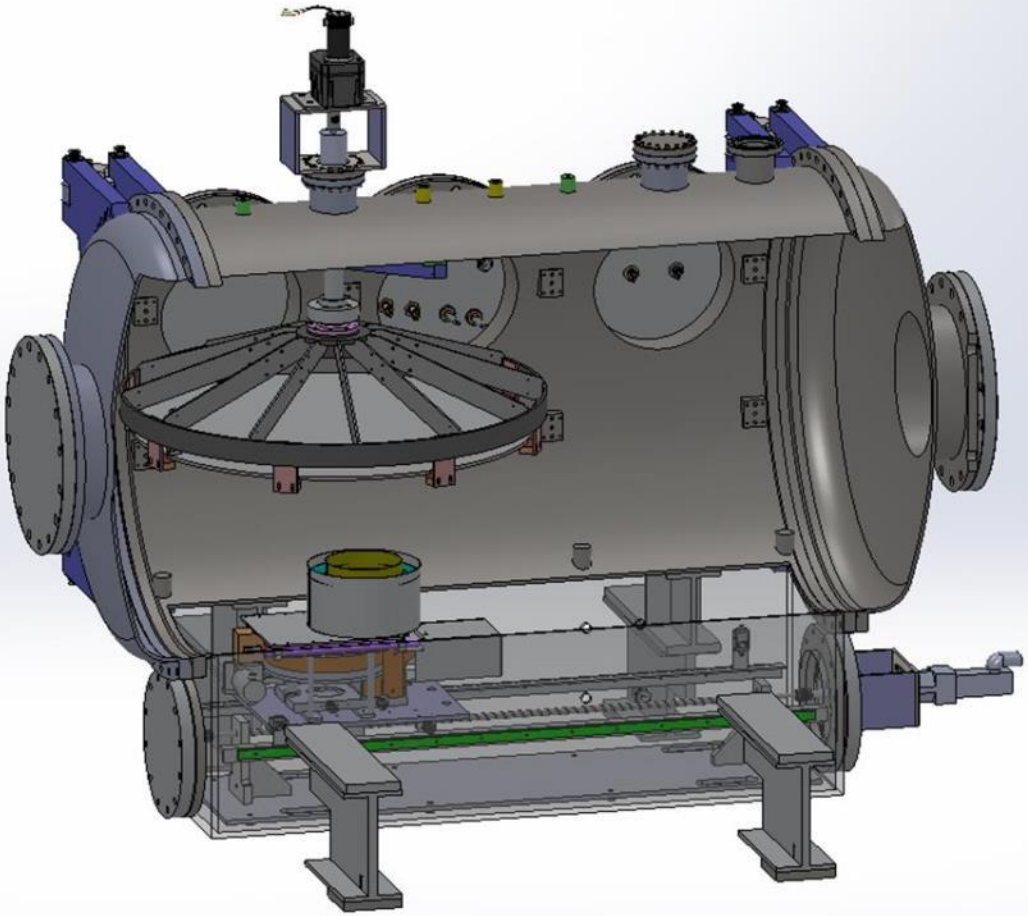
ZeCoat's 1.2-m vacuum coating chamber was completed in March, 2013 and utilizes an ion-assisted e-beam evaporation system











Overcoming Challenges

- Silicon Spitting
  - A spitting event is when molten silicon explodes from the evaporation crucible potentially damaging the silicon clad surface.
- Arcing
  - Arcs (or high voltage discharges within the chamber) cause computer faults and can damage integrated circuits (IC). Arcing is more prevalent in a Si deposition process then when coating metals and dielectrics.

Solving the Si Spitting Problem

- ZeCoat has solved the Si spitting problem with a proprietary method of ‘pre-conditioning’ the Si starting materials
- The current drawback to the preconditioning process is performed in the vacuum chamber and requires a significant amount of valuable chamber time
  - Solution: a small dedicated vacuum system for conditioning materials solves this problem

Arcing and Silicon

- The semi-conductive nature of Si causes arcing problems when combined with high voltage from the electron gun and ionized gases from the ion gun.
- Arcing begins after several hours of continuous deposition, as the chamber becomes more and more contaminated with silicon.

Overcoming Arcing Problems

- Designed and installed new shielding over the electron emitter assembly
- Added a 90's vintage ion gauge controller for monitoring chamber pressure and replaced the mass flow controllers with needle valves (simplify system by reducing # of IC's)
- Installed relays between the computer system and process sensors within the chamber, to isolate the computer from arcing interference
- Wrote new motion control software to detect false signals due to arcing and reset the computer system seamlessly
- Selected IAD processing conditions that utilize the lowest pressures

Lesson: New, state-of-the-art equipment isn't always "better"

- More integrated circuits means more things to be damaged by arcing
- Several IC's have been blown in multiple pieces of equipment (particularly the displays on power supplies and controllers)

Table of Phase I Results

					Evap Rate			IAD			
Test #	Thickness	Deflection	Stress	Stress Sign	Zone 1	Zone 2	Zone 3	volts	current	Base Pressure	NOTES
	(microns)	(microns)	Mpa		(A/sec)	(A/sec)	(A/sec)	(V)	(amps)	(torr)	
WO2009	0.37	0.45	103	tensile							
WO2010	0.23	0.2	72	comp							
WO2011	0.31	0.3	80	comp							
WO2012	0.32	0.2	52	comp							
WO2013	0.3	0.45	126	comp							
WO2014	0.34	0.1	24	comp							
WO2015	0.32	0.5	130	comp							
WO2016	0.28	0.2	60	tensile							
WO2017	0.53	0.19	30	tensile							
WO2018	2.1	2.1	84	tensile							
WO2019	2.6	4.7	>150	tensile							

Proprietary Data

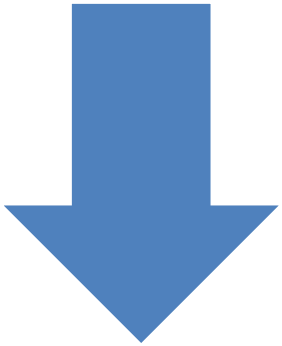
Pending Phase I Results (early November)

- Polishing results
- Net stress for thick laminates
- Coating removal tests

Compressive Stress versus Ion Voltage and Argon Partial Pressure

- Higher compressive stress was achieved with lower Ar ion potential (lower anode voltage)
- Lower anode voltages require higher argon gas flow for a given anode current (higher pressures and shorter mean free path); this is because the ion gun is less efficient at producing ions at lower anode voltages
- Shorter mean free path means more arcing problems
- Conclusion; For now, use higher anode voltage and lower pressures at the expense of slower deposition rates

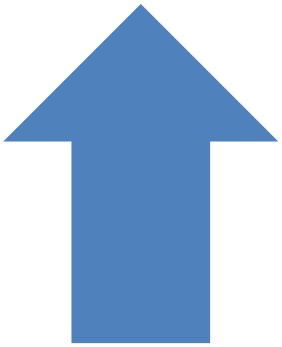
UV Mirrors Require A Highly Polishable Cladding



10 & 100-micron silicon coating

5 angstroms RMS

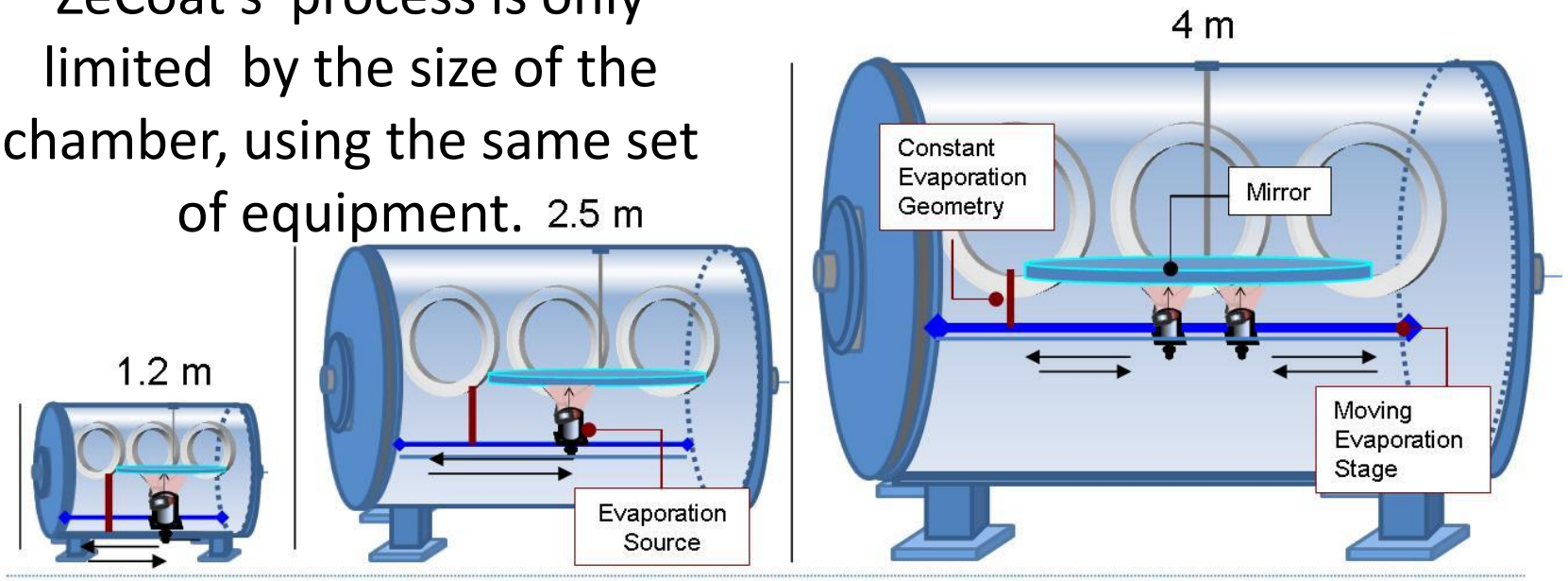
100 to 2000-angstroms RMS initial surface roughness

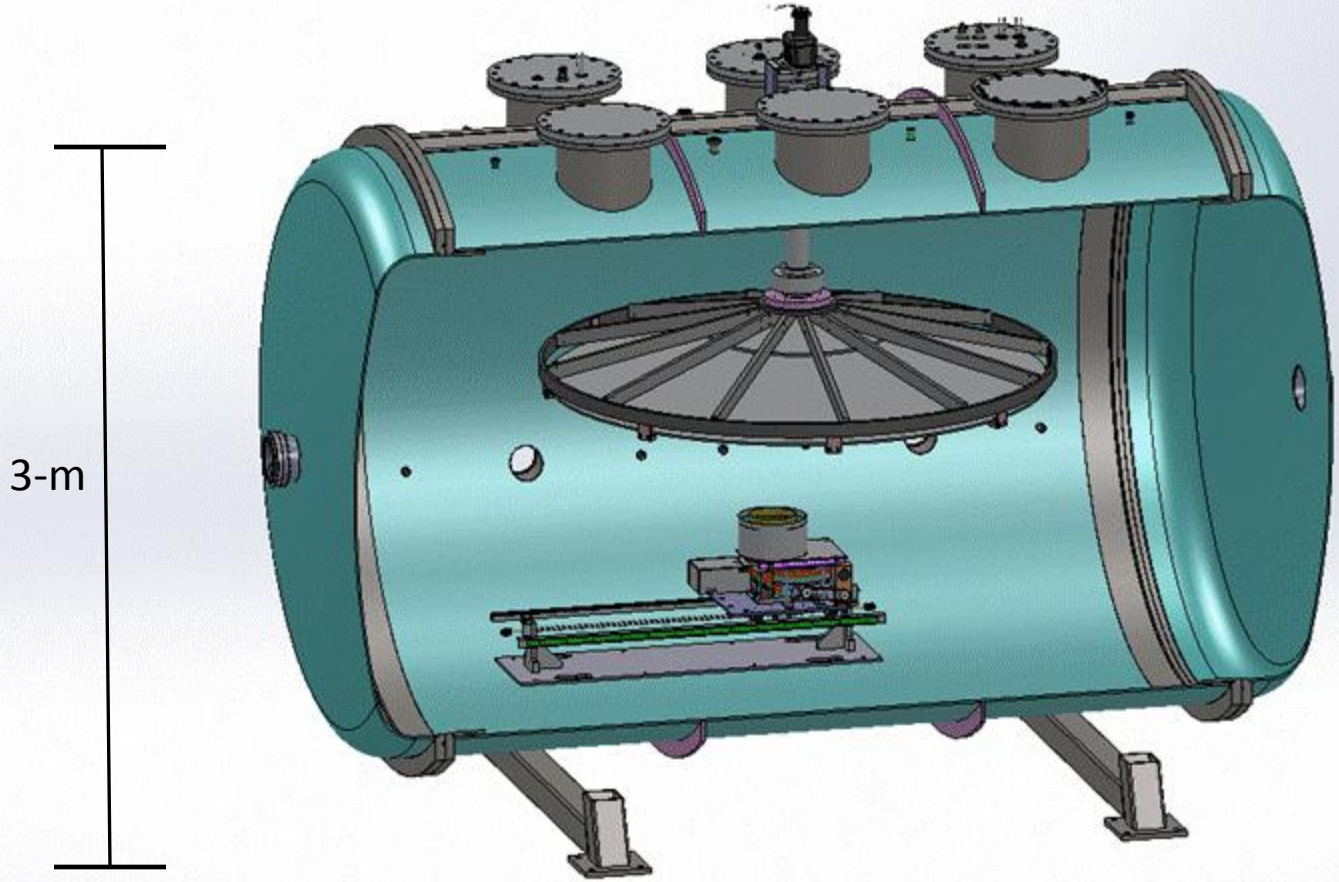


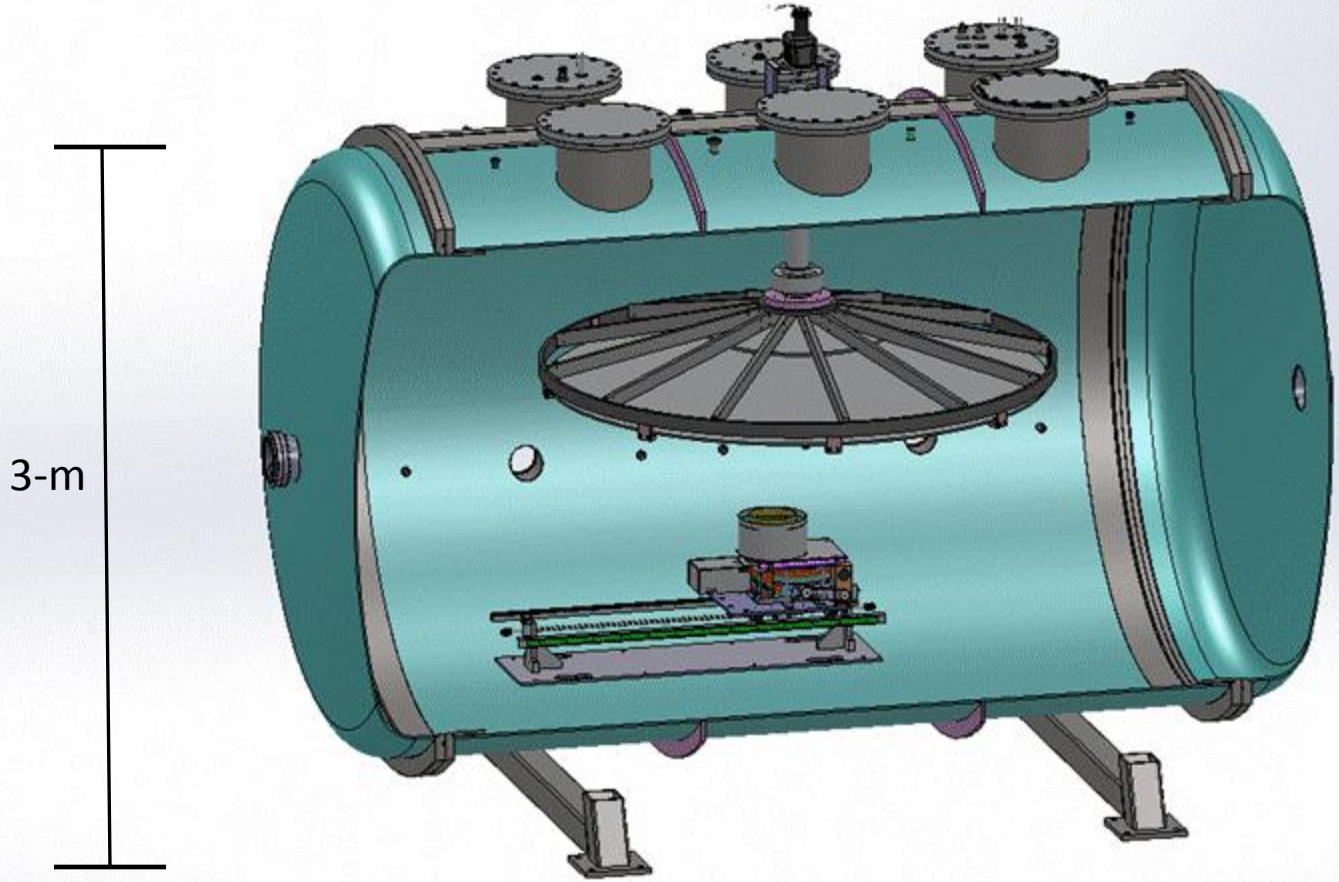
Which combinations of initial substrate surface roughness and coating thickness will result in the ability to create a super-polish?

Process Scalability

ZeCoat's process is only limited by the size of the chamber, using the same set of equipment.




3-m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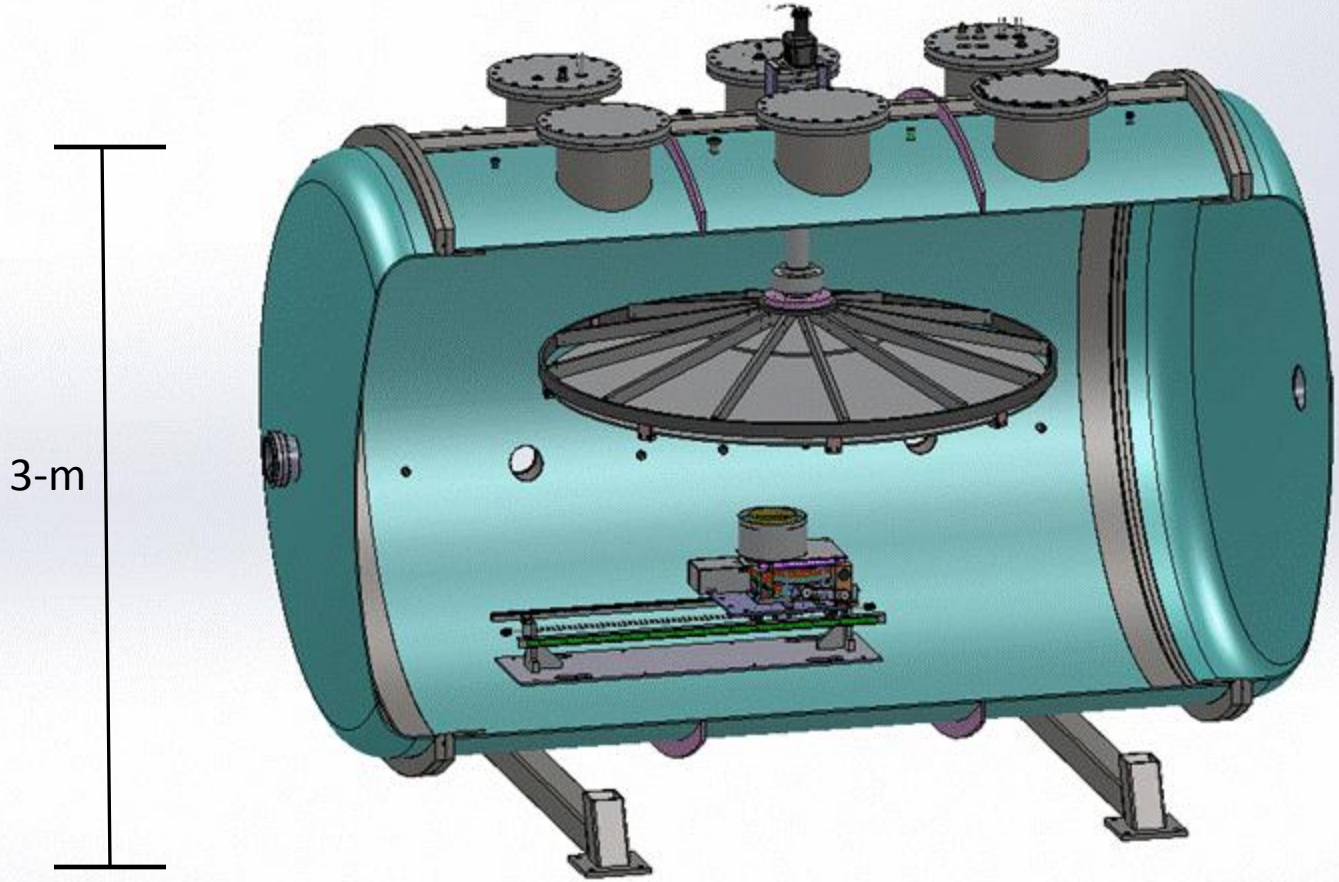
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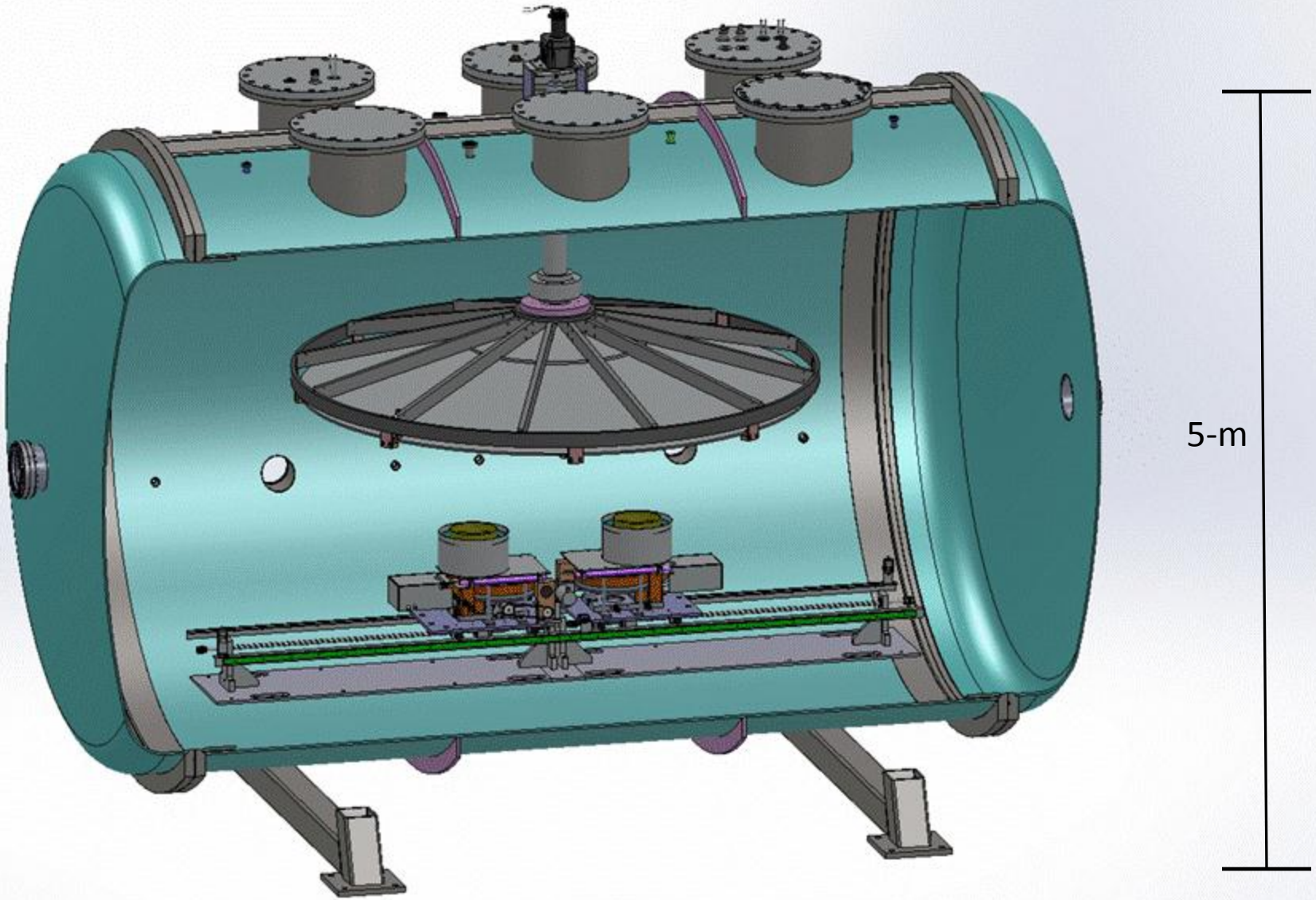
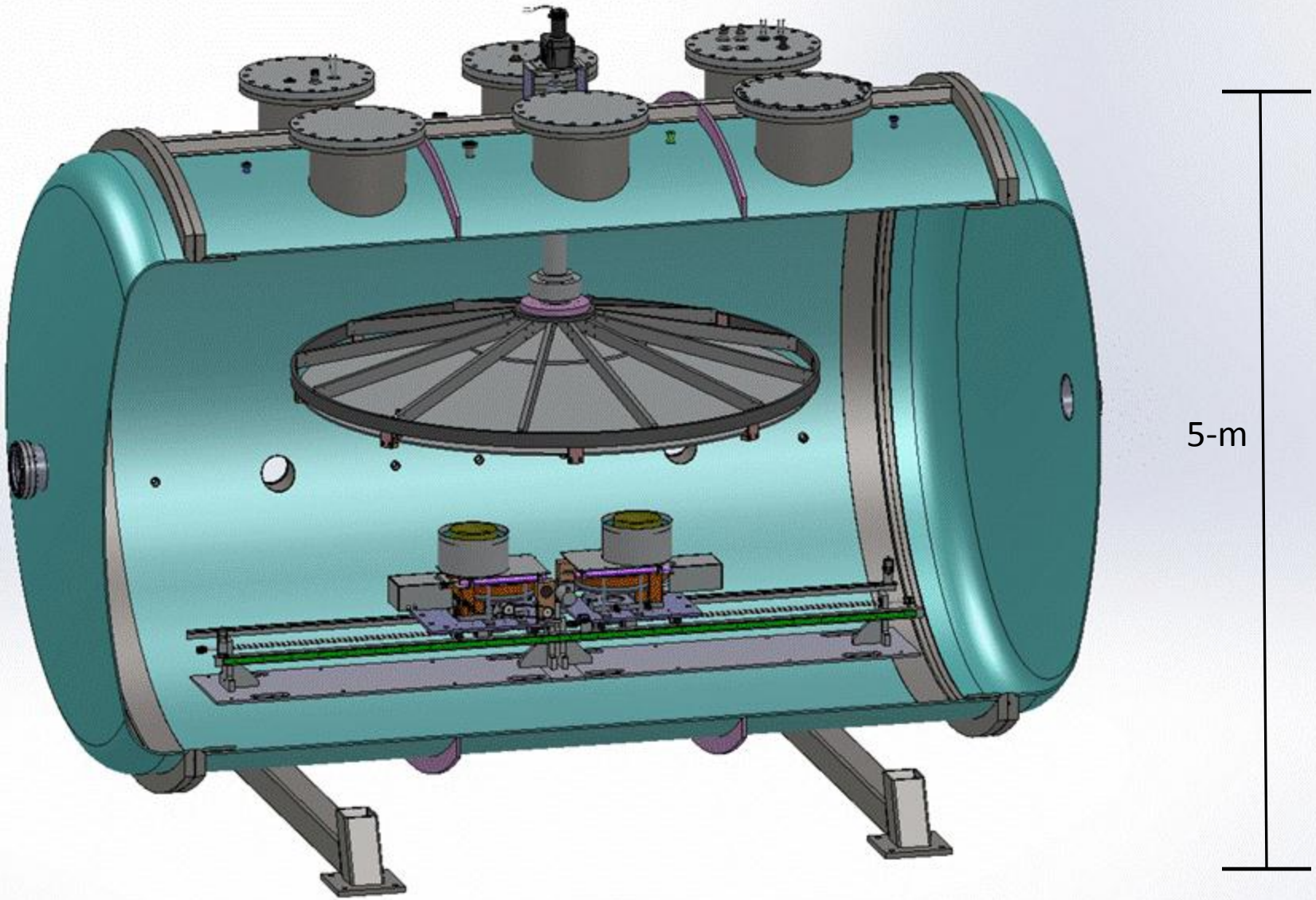
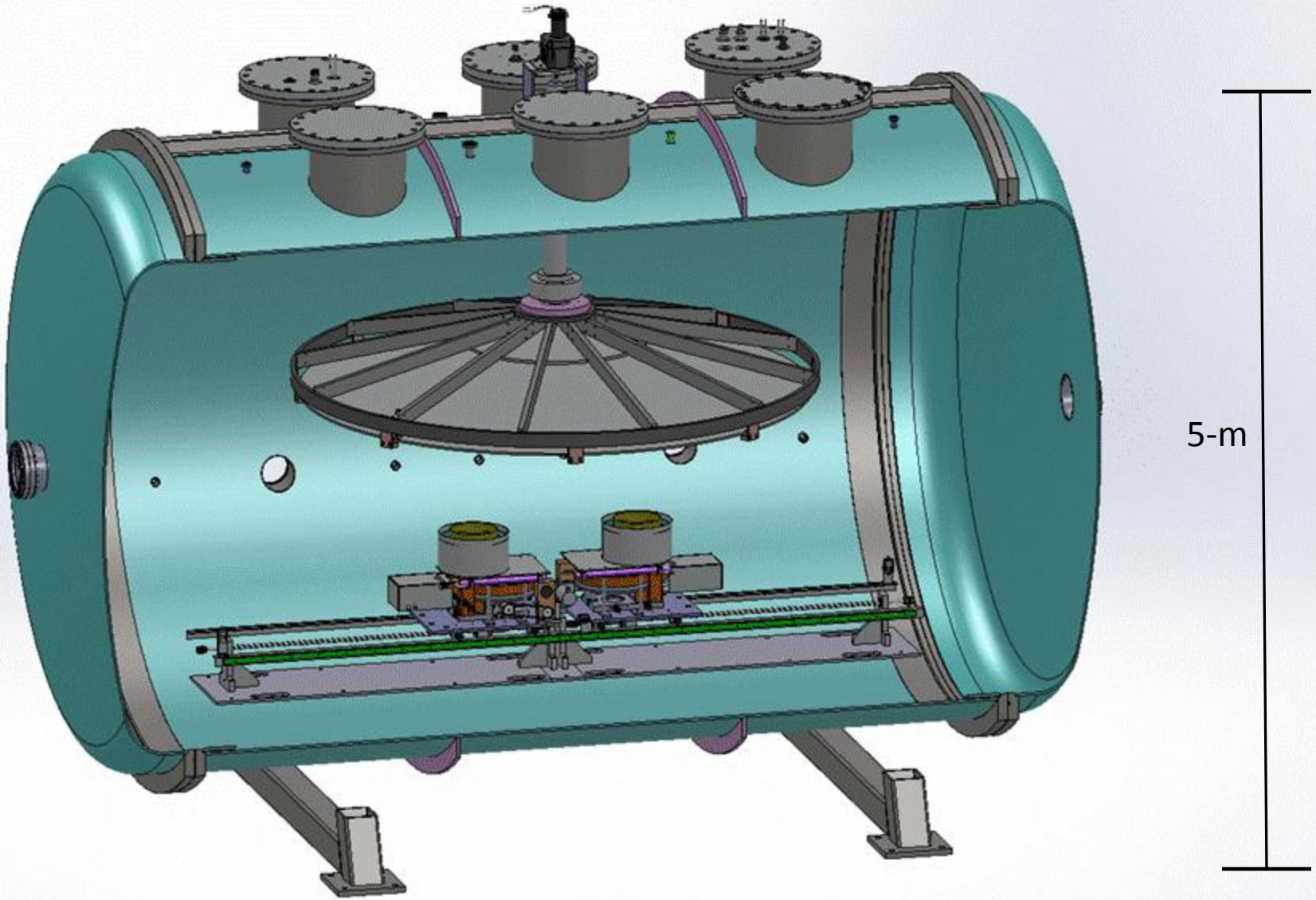

5-m


5-m


5-m

Keys to Demonstrating Phase I Feasibility

- The ability to produce single layers of tensile and compressive silicon
- The ability to fabricate a multi-layer stack of tensile and compressive layers with a low net stress
- The ability to polish silicon cladding
- Show how the process is scalable to larger sizes (up to 4-m)

Phase II's Focus - Manufacturability

Scalable

- Use same deposition equipment set in a larger chamber (2.5-m area)

Fast

- Optimize deposition rates (3x)

Reliable

- Devise system insensitive to arcing
- More automation

Phase II Production Rate Improvements

- Phase I research indicates a 3x to 6x increase in deposition rate is achievable
- A high-rate cladding process would open up markets by allowing ZeCoat to compete with CVD silicon cladding for smaller optics
- A high-speed cladding process will make thicker coatings over larger areas affordable; goal 100-microns over 4-meter area

QUESTIONS?